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Power_shift_board_70x35_Revision_History.SchDoc

Revision History

Rev.	Rel.	Date	Author	Description	Page(s)
1.1.1	RC01	2015-11-11	XY	- Initial design	
1.1.1	**Rel**	**2015-12-12**	**XY**	**Released Version**	

Power Shift Board 75x35

[No Variations]

V1.1.1

Infineon Technologies AG

IFAT DC ATP BP ASE

Siemensstrasse 2 - 9500 Villach - Austria

05/2018

Link to Top Level Document

02 Top Level
RCLS_70x35.SchDoc

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Title	Power Shift Board 75x35		
Variant	[No Variations]	Approved	<Appr.>
Size: A3	Document Name: Power_shift_board_70x35_Revision_History.SchDoc	Rel.: REL	Rev.: V1.1.1
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Date: 8/5/2018	Time: 10:37:49 AM	SVN Revision: 6602	

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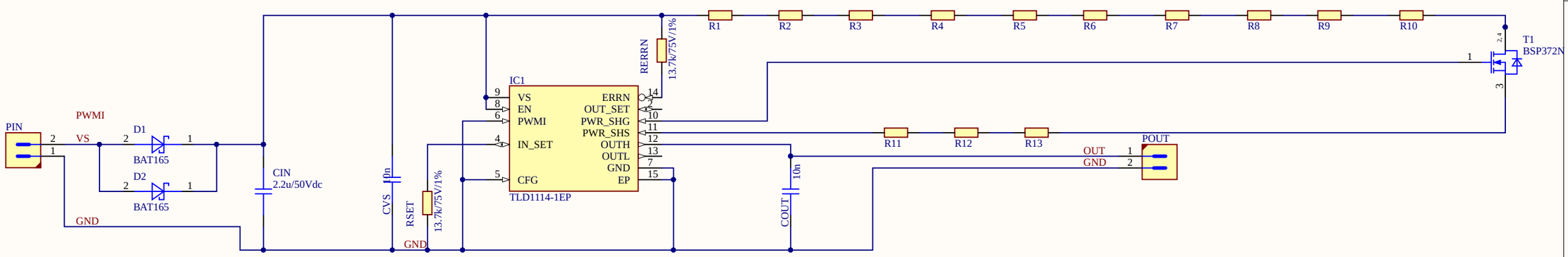
RCLS_70x35.SchDoc



Design hints/wishes

Total PCB size = 60mmx30mm => Size specified/agreed with customer
Place CVS, RSET, SJCFG, COUT, SJOUTL, SJOUTH close to IC1; GND loop to IC GND should be also short
All components on top layer as indicated in draft placement
All Vias should be covered with soldermask (white - top/bottom as in Basic+ Mid End board) to ensure clean position print
Standard two layer FR4 PCB (35um copper)
Blue silkscreen (can this be set in Altium somewhere?)
Flood bottom layer and other free space with GND
Cooling planes on Top/bottom around RPWRxxxx + via stitching
Thermal vias under IC1 to connect to GND plane for cooling
Position print Top: Component names, + connector designators
Position print Bottom:
- IFX Logo
- Power Shift
- Thermal evaluation board
- 60mm*30mm V1.0 2017.09

Total board current <400mA
OUTx traces should be on top layer with GND underneath
Place CIN close to connector

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